Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Withdrawn) A semiconductor device comprising:

a transistor on a semiconductor substrate; and

contact portions for connecting a lower layer and an upper layer arranged in plural lines.

2. (Withdrawn) A semiconductor device comprising:

a first transistor on a semiconductor substrate;

first contact portions for connecting a lower layer and an upper layer in the first transistor;

a second transistor on the semiconductor substrate; and

second contact portions for connecting a lower layer and an upper layer in the second transistor,

wherein numbers of the first contact portions and the second contact portions are different.

3. (Withdrawn) The semiconductor device according to claim 2, wherein the first contact portions are arranged in one line, and the second contact portions are arranged in plural lines.

4. (Withdrawn) The semiconductor device according to claim 2, wherein the second transistor further comprises:

a source/drain region formed to be adjacent to a gate electrode; and

a semiconductor region constituting a channel formed under the gate electrode.

5. (Withdrawn) The semiconductor device according to claim 4, wherein the second transistor further comprises a low concentration region of the same conductive type as the conductive type of the source/drain region, formed to connect to the source/drain region and to contact the semiconductor region under the gate electrode of the second transistor.

6. (Withdrawn) The semiconductor device according to claim 4, wherein the second transistor further comprises a low concentration region of the same conductive type as the conductive type of the source/drain region, formed being extended shallowly to the semiconductor region to connect to the source/drain region and to contact the semiconductor region under the gate electrode of the second transistor.

7. (Withdrawn) The semiconductor device according to claim 1, wherein the contact portions are provided for connecting to the source/drain region.

8. (Withdrawn) The semiconductor device according to claim 1, wherein the contact portions are provided for connecting to the lower layer wiring and the upper layer wiring.

9. (Withdrawn) The semiconductor device according to claim 1, wherein a conductive film is buried in the contact portions.

10. (Withdrawn) A semiconductor device comprising:

a low concentration opposite conductive type source/drain region formed in one conductive type semiconductor;

a high concentration opposite conductive type source/drain region formed in the low concentration opposite conductive type source/drain region;

a gate electrode formed on the semiconductor through gate oxide film;

a one conductive type semiconductor region formed under the gate electrode and constituting a channel placed between the source/drain region;

contact portions contacting arranged in plural lines; and

a source/drain electrode connected to the source/drain region through the contact portions.

11. (Withdrawn) A method of manufacturing a semiconductor device including transistors on a semiconductor substrate, the method comprising a step of forming contact portions for connecting a lower layer and an upper layer in plural lines.

12. (Withdrawn) A method of manufacturing a semiconductor device including a first transistor and a second transistor on a semiconductor substrate, the method comprising the steps of:

forming first contact portions for connecting a lower layer and an upper layer in the first transistor;

forming second contact portions for connecting a lower layer and an upper layer in the second transistor,

wherein numbers of the first contact portions and the second contact portions are different.

13. (Withdrawn) The method of manufacturing a semiconductor device according to claim 12, wherein the first contact portions are arranged in one line, and the second contact portions are arranged in plural lines.

14. (Withdrawn) The method of manufacturing a semiconductor device according to claim 11, wherein the contact portions are provided for connecting to the source/drain region.

15. (Withdrawn) The method of manufacturing a semiconductor device according to claim 11, wherein the contact portions are provided for connecting to the lower layer wiring and the upper layer wiring.

16. (Withdrawn) A method of manufacturing a semiconductor device including a gate electrode on a one conductive type semiconductor through gate oxide film, the method comprising the steps of:

forming a low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity in the semiconductor;

forming a low concentration opposite conductive type region connecting to the low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a high concentration opposite conductive type source/drain region in the low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a one conductive type body region dividing the opposite conductive type region under the gate electrode by ion-implanting one conductive type impurity; and

forming contact portions for connecting to the source/drain region in plural lines through an interlayer insulating film covering the gate electrode.

17. (Withdrawn) The method of manufacturing a semiconductor device according to claim 11, further comprising a step of burying a conductive film in the contact portions.

18 - 20. (Canceled)

21. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on the gate oxide film;

a source/drain region formed in the semiconductor substrate and disposed adjacent to the gate electrode;

a lower layer wiring connected to the source/drain region with contact;

an interlayer insulating film covering the lower layer wiring;

a via hole formed in an interlayer insulating film; and

an upper layer wiring ~~having a pad portion~~, disposed over the interlayer insulating film and connected to the lower layer wiring through the via hole,

wherein the upper layer wiring and the lower layer wiring are arranged under a pad portion and in areas other than under the pad portion, and

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion.

22. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on gate oxide film;

a source/drain region formed in the semiconductor substrate and disposed adjacent to the gate electrode;

a semiconductor region formed under the gate electrode comprising a channel;

a low concentration region of the same conductivity type as the source/drain region formed under the gate electrode so as to connect to the source/drain region and to contact the semiconductor region;

interlayer insulating film disposed over the gate electrode and the gate oxide film;

a lower layer wiring disposed in the interlayer insulating film and coupled to the source/drain region; and

an upper layer wiring disposed over the interlayer insulating film and coupled to the lower layer wiring through a hole in the interlayer insulating film.

23. (Previously Presented) A semiconductor device according to claim 21, further comprising:

a semiconductor region formed under the gate electrode, said region comprising a channel, wherein the low concentration region extends shallowly to a surface layer under the gate electrode to connect to the source/drain region and to contact the semiconductor region.

24 - 27. (Canceled)

28. (Previously Presented) The semiconductor device according to claim 21, wherein the interlayer insulating layer is provided with additional holes to couple the upper wiring to the lower layer wiring.

Claims 29-30. (Canceled)

31. (Previously Presented) The semiconductor device according to claim 21, further comprising a semiconductor region formed under the gate electrode and constituting a channel.

32. (Previously Presented) The semiconductor device according to claim 31, further comprising a bump electrode provided at the pad portion.

33. (Previously Presented) The semiconductor device according to claim 21, further comprising a bump electrode provided at the pad portion.

34. (Currently amended) A semiconductor device comprising:

a lower layer wiring;

an interlayer insulating film covering the lower layer wiring;

a via hole formed in the interlayer insulating film; and

an upper layer wiring ~~having a pad portion~~, disposed over the interlayer insulating film and connected to the lower layer wiring through the via hole,

wherein the upper layer wiring and the lower layer wiring are arranged under a pad portion and in areas other than under the pad portion, and

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion.

35. (Previously presented) The semiconductor device according to claim 34, wherein the interlayer insulating layer is provided with additional holes to couple the upper layer wiring to the lower layer wiring.

36. (Previously presented) The semiconductor device according to claim 34, further comprising a bump electrode provided at the pad portion.

37. (Previously presented) The semiconductor device according to claim 36, further comprising the lower layer wiring arranged below the bump electrode.

38. (New) The semiconductor device according to claim 21 wherein the pad portion comprises a bump electrode.

39. (New) The semiconductor device according to claim 34 wherein the pad portion comprises a bump electrode.